MARCO APOLINARIO

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ABOUT

Electronic Engineer interested in Hardware/Software co-design for Brain-Inspired Computing. Previous experience developing bio-plausible deep learning, computer vision applications, managing research projects and small teams.

EDUCATION

Purdue University, Graduate School of Electrical and Computer Engineering West Lafayette, IN
Ph.D. in Electrical and Computer Engineering (Expected graduation: December 2025) January 2021-Present
Advisor: Prof. Kaushik Roy – Research Topic: Brain-Inspired Computing – GPA: 3.9

National University of Engineering, School of Electrical and Electronics Engineering Lima, Peru
B.Sc. in Electronics Engineering – GPA: 3.5 – Rank: 3/28 March 2013-December 2017

RESEARCH EXPERIENCE

Purdue University – Center for Brain-Inspired Computing (C-BRIC) West Lafayette, IN
Graduate Research Assistant August 2021-Present

- Conducted research on neuro-inspired machine learning algorithms for emerging hardware technologies.
- Designed a novel ADC-Less In-memory Computing Hardware, specifically optimized for Spiking Neural Networks, employing a collaborative HW/SW co-design approach. This resulted in remarkable energy savings of 2-7x and latency reductions of 9-24x when compared to traditional architectures.
- Engineered and implemented a novel temporal local learning rule (S-TLLR) for Spiking Neural Networks, drawing inspiration from the STDP mechanism. This approach demonstrated equivalent performance to the BPTT algorithm across various time-dependent tasks with 1.3-6.6x reduction in memory usage.

Kilby Labs – Texas Instruments Dallas, TX
Systems Engineering Intern May 2023-August 2023

- Conducted research into hardware-aware neural architecture and quantization search, leveraging evolutionary optimization algorithms to facilitate the deployment of deep learning models on low-power devices.

National Institute for Research and Training in Telecommunications (INICTEL-UNI) Lima, Peru
Research Assistant in Computer Vision July 2017-December 2020

- Contributed to the development of various machine learning models for different applications, including timber species identification, underwater acoustic inversion, satellite cloud segmentation, and river level estimation.
- Integrated machine learning algorithms into low-power electronic systems to enable real-time inference capabilities for precision agriculture applications.
- Innovated by proposing a lightweight CNN model designed for recognizing timber species in microscope images, achieving accuracy rates exceeding 90%, even in scenarios with open-set conditions.
- Obtained three software copyrights, covering applications in remote sensing and health monitoring.
- Shared insights through scholarly contributions, including one journal paper and three conference papers.

RELEVANT RESEARCH PROJECTS

Hardware/Software co-design of In-memory Computing for Spiking Neural Networks December 2021-Present

- Designed energy-efficient In-memory Computing hardware for spiking neural networks (SNN) to deploy such models for real-time edge applications achieving low latency and energy consumption.

Open-Set Recognition of Peruvian Timber Species January 2018-March 2020

- Produced one low-power field-deployable electronic prototype to perform open-set recognition of 16 Peruvian timber species in real-time with high accuracy based on a lightweight convolutional neural network.

Software for Cloud Segmentation of PERUSAT-1 Multispectral Satellite Images July 2019-December 2019

- Developed a software product for the Space Agency of Peru (CONIDA) to generate accurate cloud masks over PERUSAT-1 images (high-resolution multispectral satellite images) based on deep learning models.

SELECTED PUBLICATIONS

- Chowdhury, S., A. Kosta , D. Sharma , **M. Apolinario**, and K. Roy (2024). "Unearthing the Potential of Spiking Neural Networks". In Design, Automation & Test in Europe Conference & Exhibition (DATE).
- **Apolinario, M.** and K. Roy (Under Review, 2024). "S-TLLR: STDP-inspired Temporal Local Learning Rule for Spiking Neural Networks".
- Biswas, S., A. Kosta, C. Liyanagedera, **M. Apolinario**, and K. Roy (2024). "HALSIE – Hybrid Approach to Learning Segmentation by Simultaneously Exploiting Image and Event Modalities". In Proceedings of the IEEE/CVF Winter Conference on Applications of Computer Vision (WACV).
- **Apolinario, M.**, A. Kosta, U. Saxena, and K. Roy (2023). "Hardware/Software co-design with ADC-Less In-memory Computing Hardware for Spiking Neural Networks". IEEE Transactions on Emerging Topics in Computing.
- Kosta, A., **M. Apolinario**, and K. Roy (2023). "ANN vs SNN vs Hybrid Architectures for Event-based Real-time Gesture Recognition and Optical Flow Estimation". In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR) Workshops.
- **Apolinario, M.**, D. Urcia, and S. Huaman (2019). "Open Set Recognition of Timber Species Using Deep Learning for Embedded Systems". In IEEE Latin America Transactions.
- **Apolinario, M**., S. Huamán, G. Morales, and D. Diaz (2019). "Estimation of 2D Velocity Model using Acoustic Signals and Convolutional Neural Networks". In IEEE INTERCON.
- **Apolinario, M**., S. Huamán, and G. Orellana (2018). "Deep Learning Applied to Identification of Commercial Timber Species from Peru". In IEEE International Conference on Electronics, Electrical Engineering and Computing.

RELEVANT COURSEWORK

- **Electronics courses:** Computer Architecture (Fall'23), System on Chip Design (Fall'22), Analog CMOS Design (Fall'22), Advanced VLSI Design (Spring'22), MOS VLSI Design (Fall'21), Solid State Devices (Spring'21).
- **Computer Science courses:** Applied Quantum Computing (Spring' 23), Optimization for Deep Learning (Fall'23), Computational Methods in Optimization (Spring'22), Artificial Intelligence (Fall'21).
- **Relevant Course Projects:**
  - **Hardware accelerator for Spiking Neural Networks on FPGA [ECE695 – System on Chip Design]**
    - Designed, implemented, and evaluated an extended custom instruction for Nios II and a custom hardware module to accelerate the inference of a SNN for sequential image classification obtaining an improvement of 30x in latency.
    - Skills: Verilog, Intel FPGA design, and system-on-chip (SoC) design.
  - **Multi-bit dot-product operation with SRAM-cells [ECE695 – Advanced VLSI Design]**
    - Implemented an analog-like in-memory multi-bit dot-product engine using standard 8T-SRAM cells.
    - Skills: Cadence Virtuoso, mixed-signal design, and corner analysis.

AWARDS

- **Fully funded Graduate Peruvian Fellowship "Beca Generacion del Bicentenario" (2020):** Awarded to outstanding young Peruvian professionals by the Peruvian Ministry of Education.
- **"Julio Urbina Arias" Award (2017):** Awarded to outstanding student member in research and projects of the IEEE Student Branch at the National University of Engineering, Lima, Peru.

TECHNICAL STRENGTHS

Programming Skills: Python, C++, VHDL/Verilog, Pytorch, Tensorflow/Keras.
Software and Additional Applications: Cadence Virtuoso, Quartus Prime, and Eagle PCB.
Spoken Languages: Spanish (Native), English (Professional working proficiency).